Cache Storage Channels **Alias-driven Attacks**

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Hamed Nemati
Christoph Baumann

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Presented by:
Paul Murley
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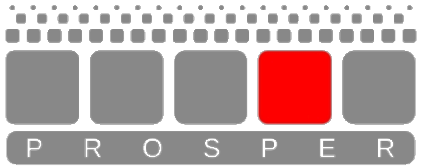
This is a modified version of the original slide deck presented by the authors.

Formally Verified Platforms



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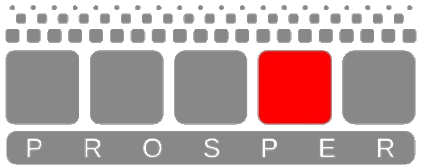

Caches Excluded from the analysis

Formally Verified Platforms

seL4
Security. Performance. Proof.

Microsoft
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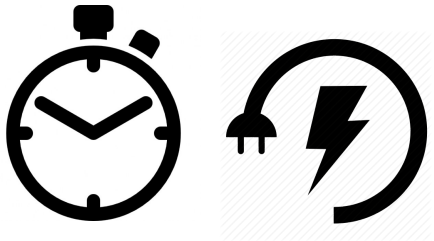

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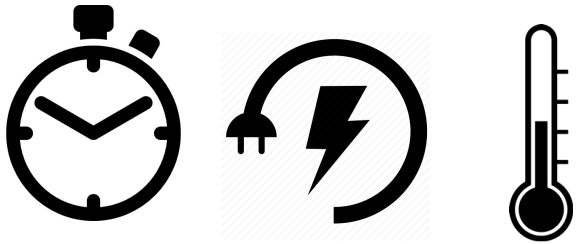

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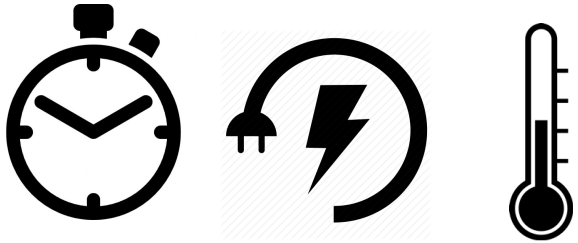

Models should be Sound

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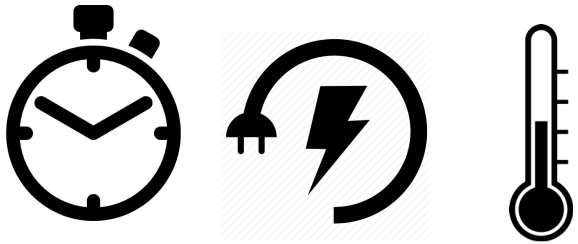
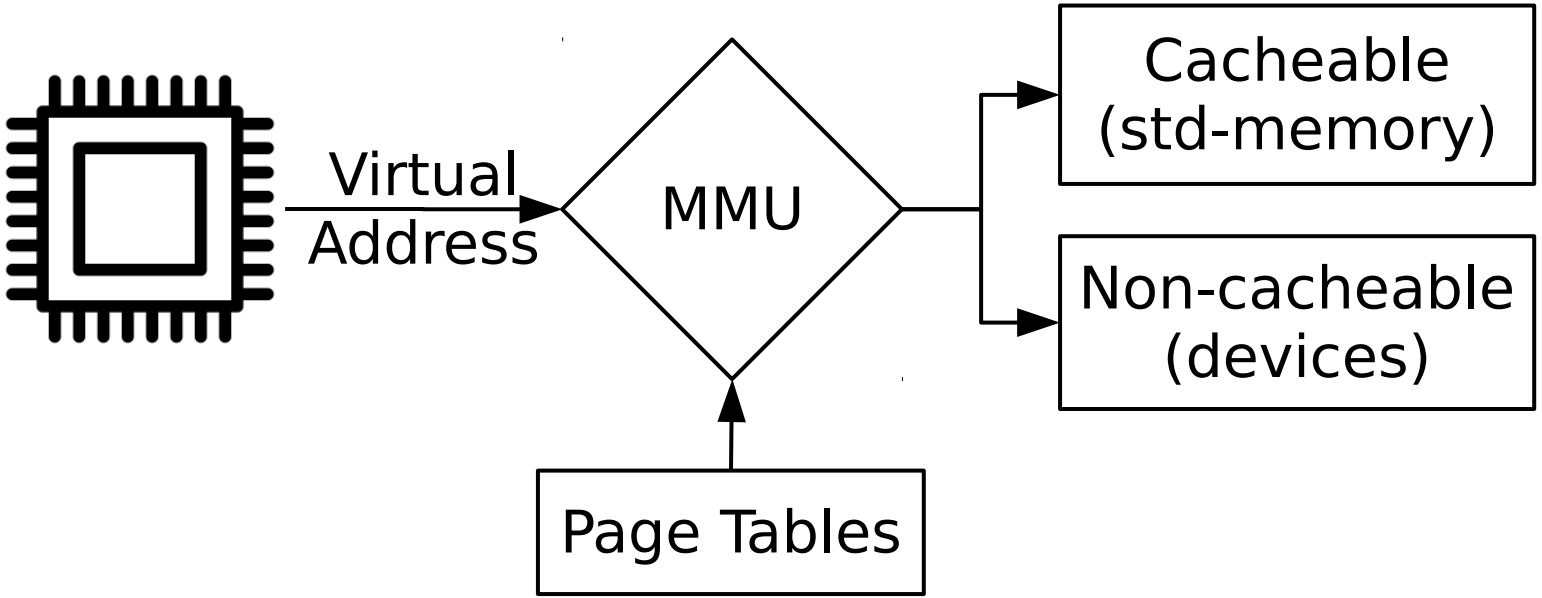


Models should be Sound

Storage Channels can invalidate results



Incoherent Cache Behaviors

Mismatched cacheability attributes

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Please, do not do this

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Incoherent Cache Behaviors

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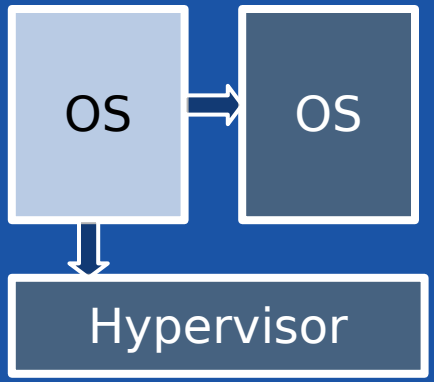
Incoherent Cache Behaviors

ARM-terminology: **unexpected cache hit**

if the data cache reports a hit on a memory location that is marked as non-cacheable, the cache might access the memory disregarding such hit.



Scenarios

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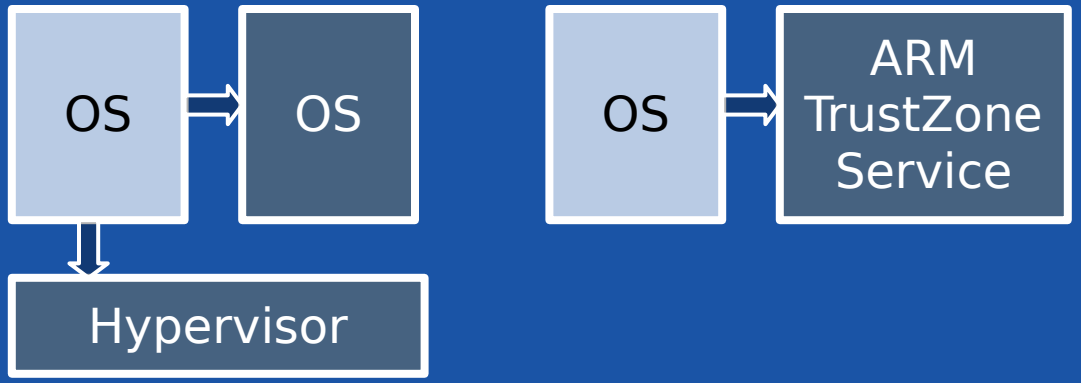

Attacker

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Victim

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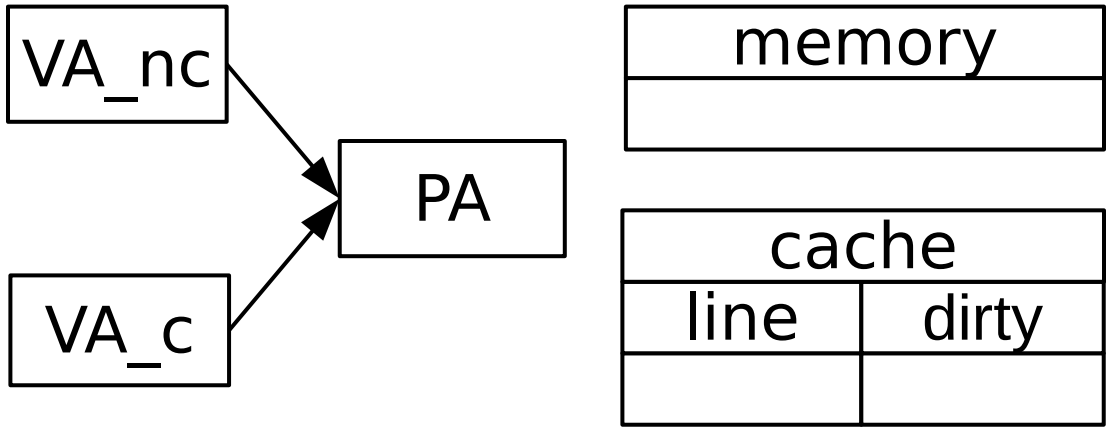

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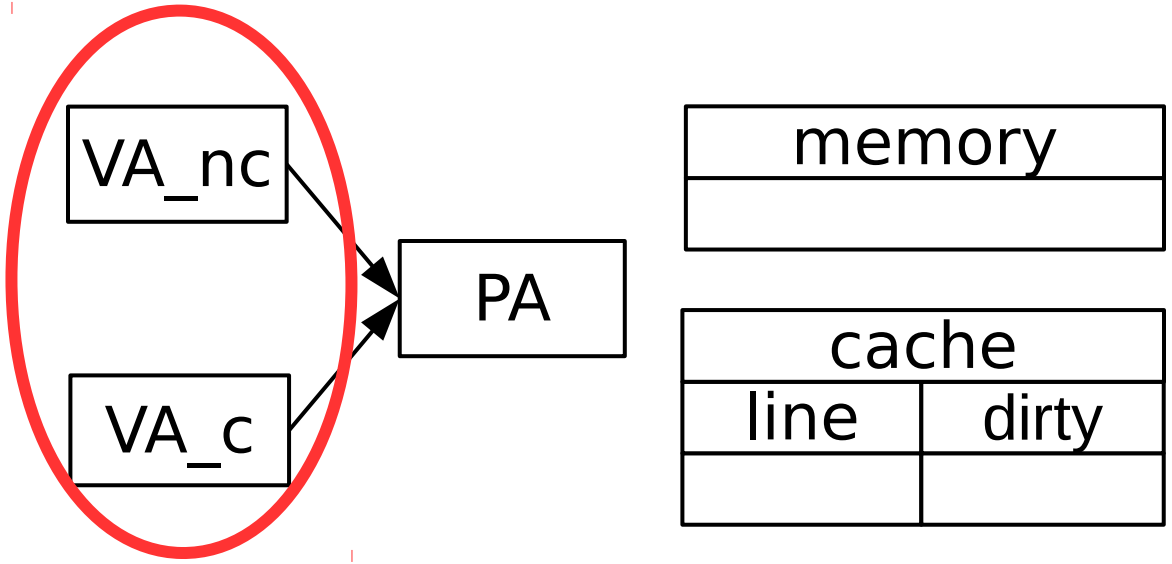

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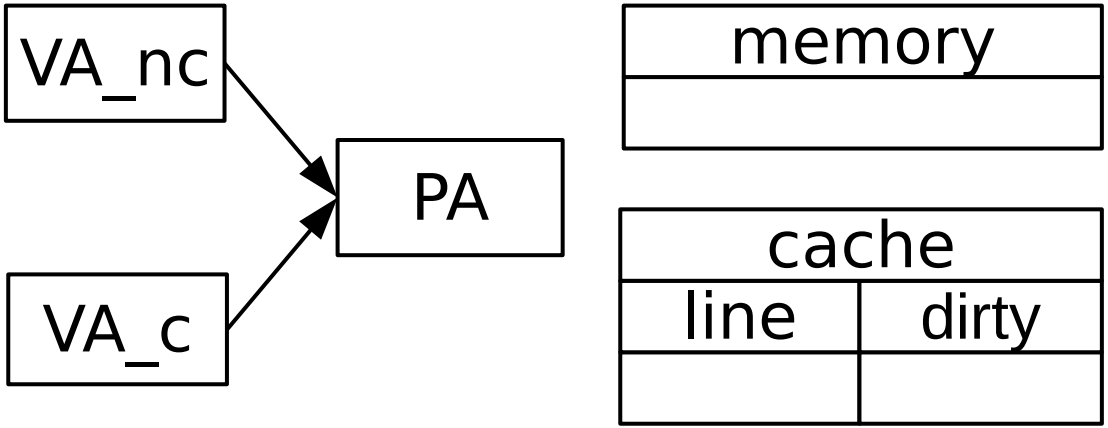

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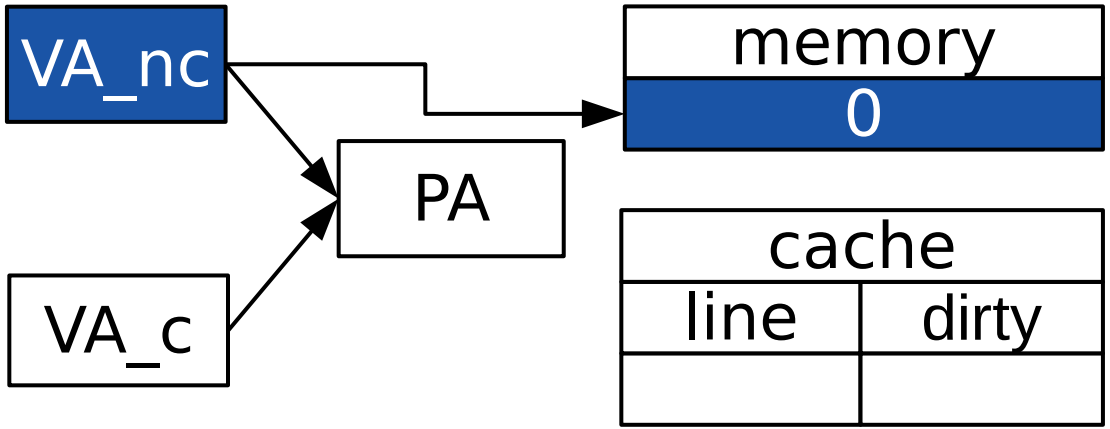

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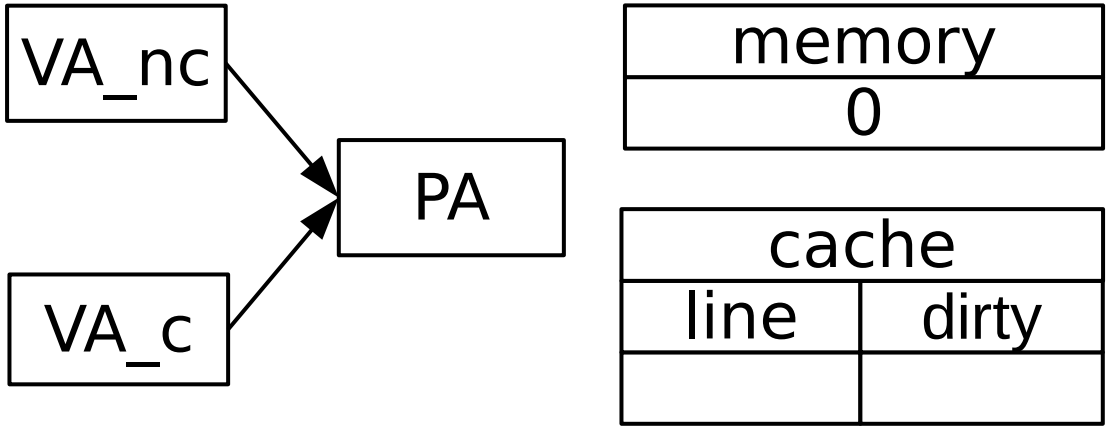

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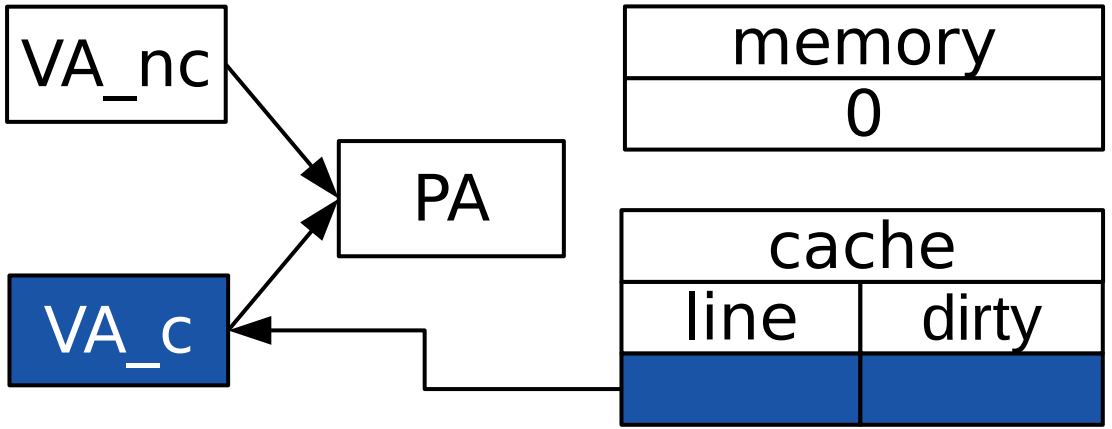

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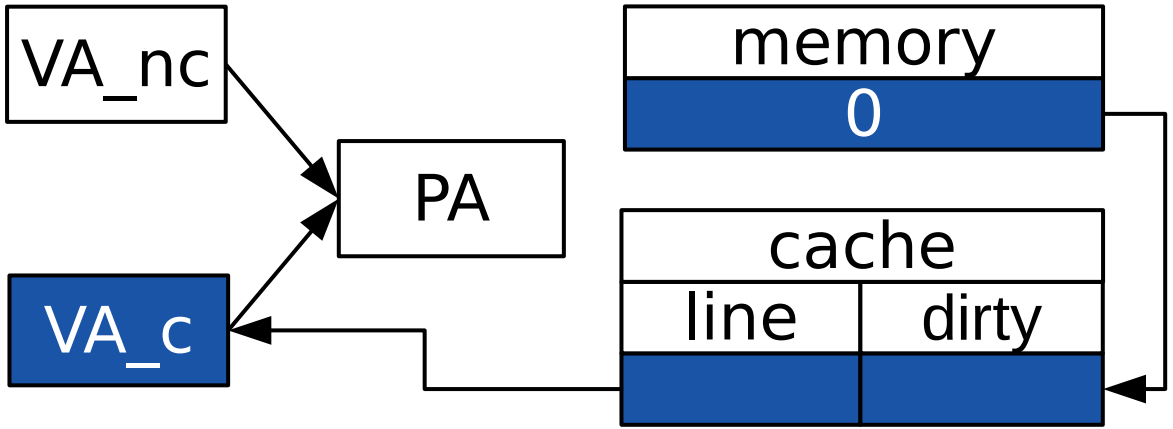

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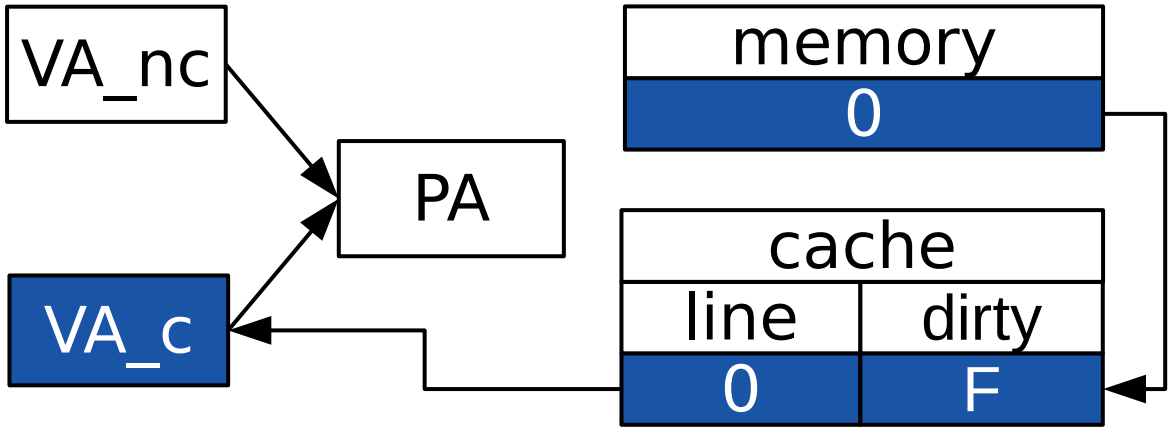

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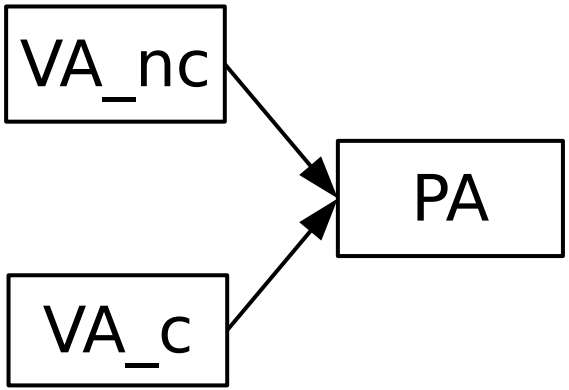

memory
0

cache	
line	dirty
0	F

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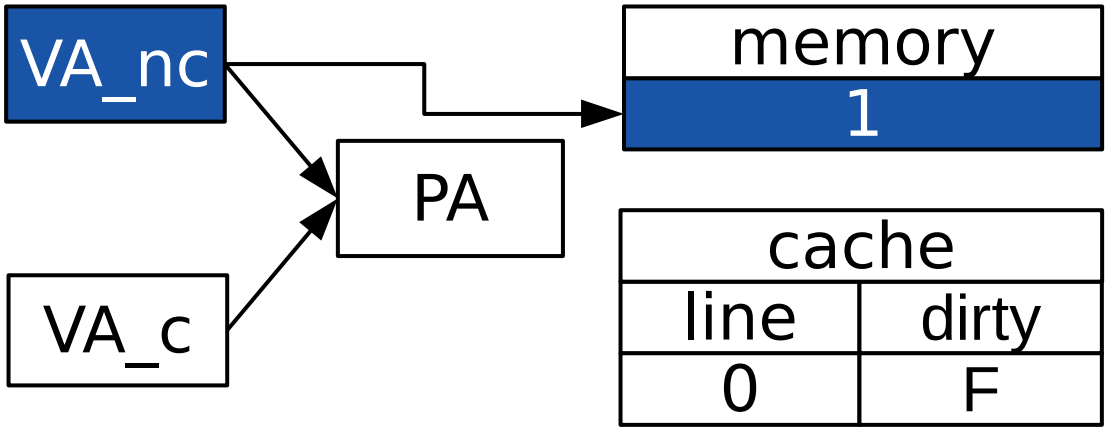

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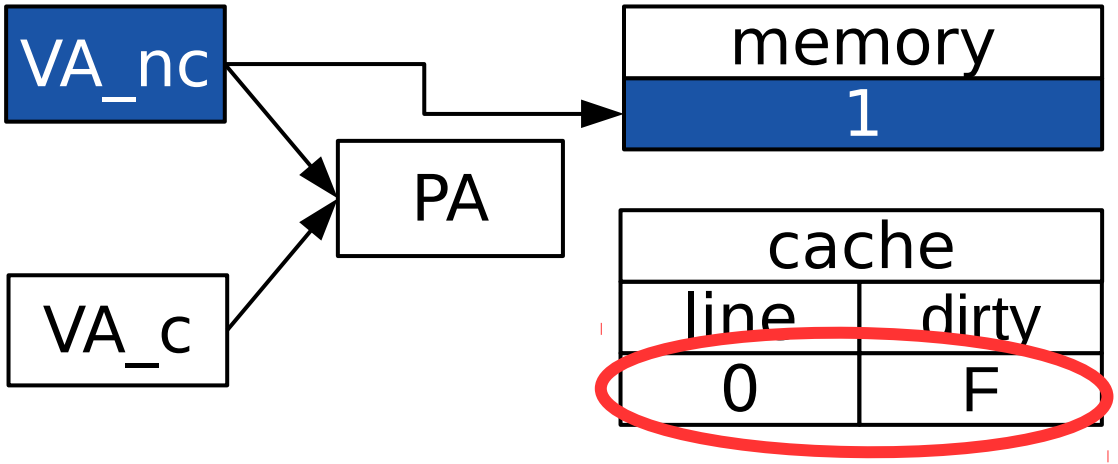

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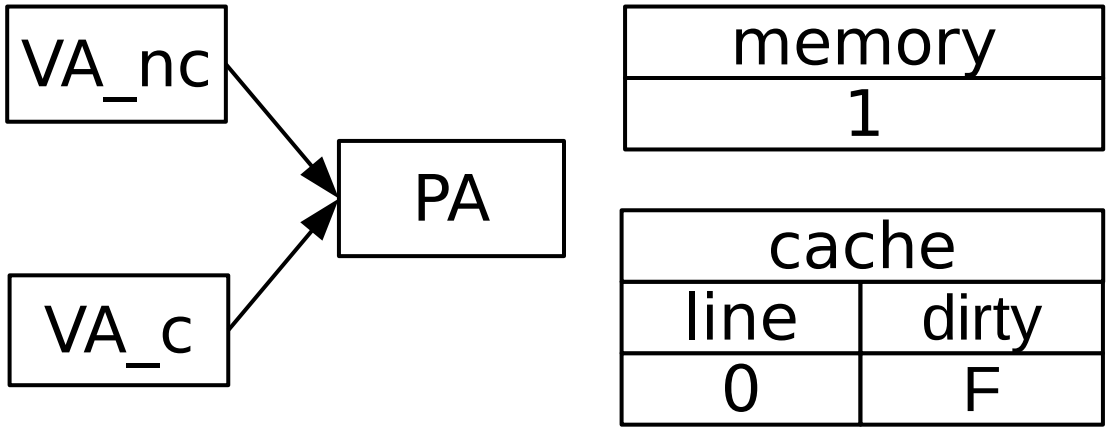

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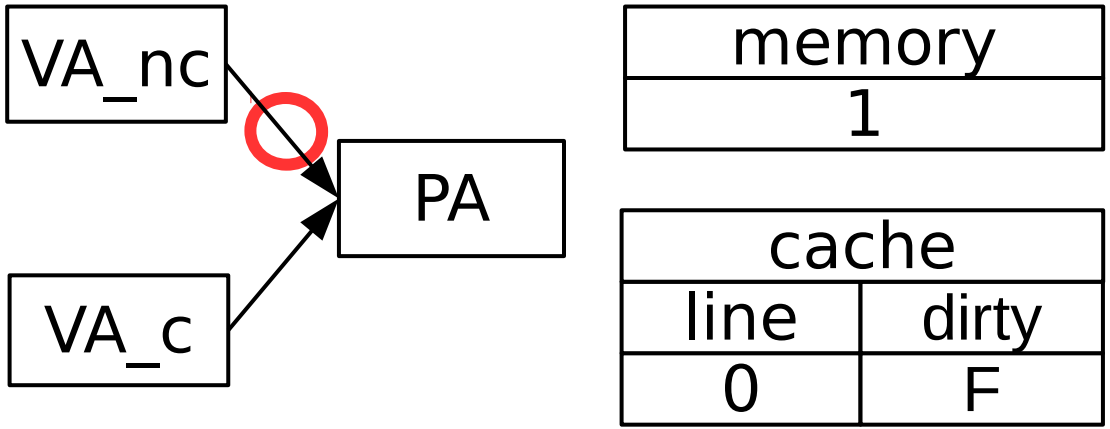

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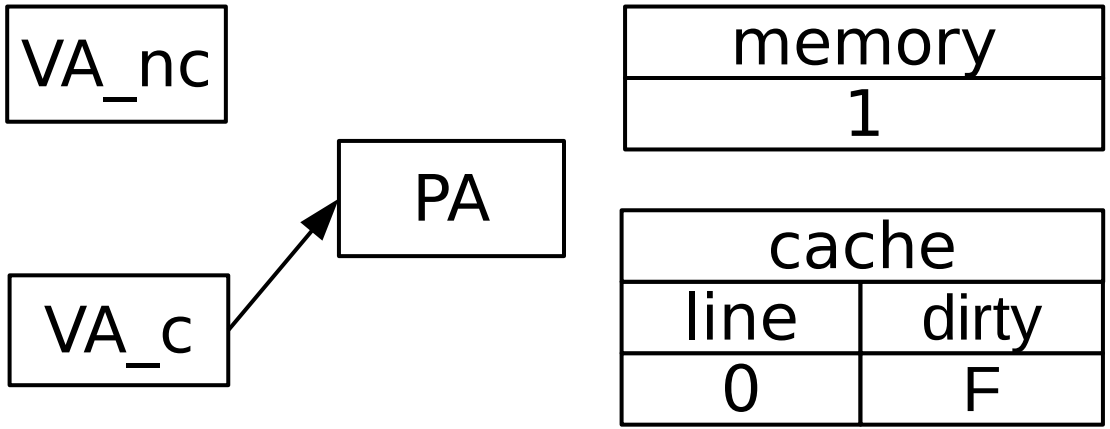

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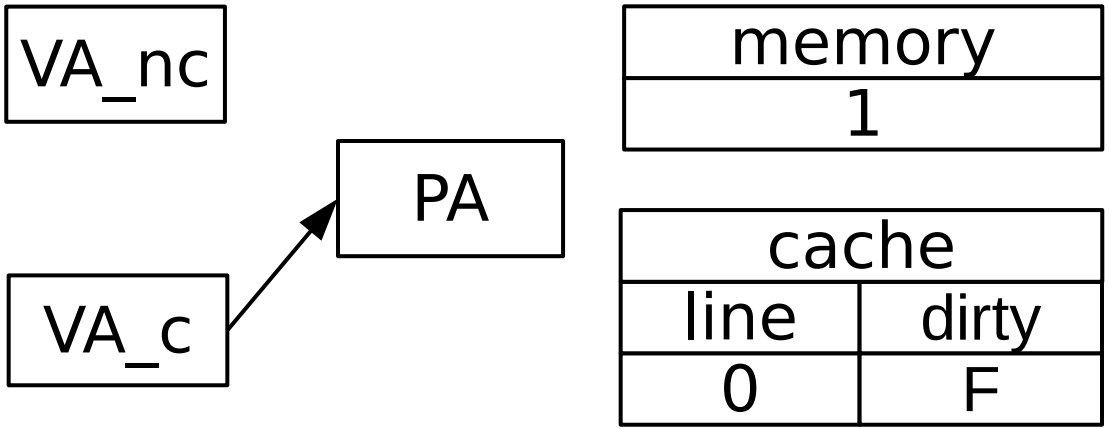

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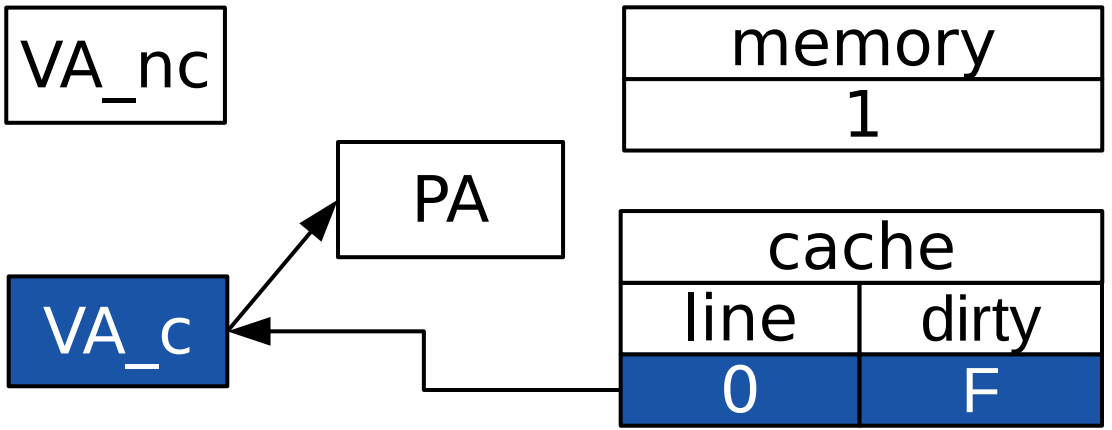

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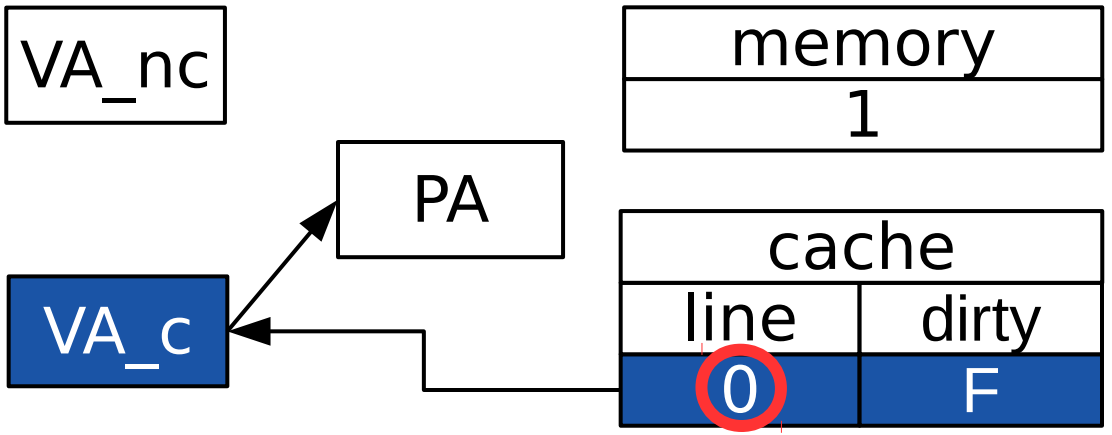

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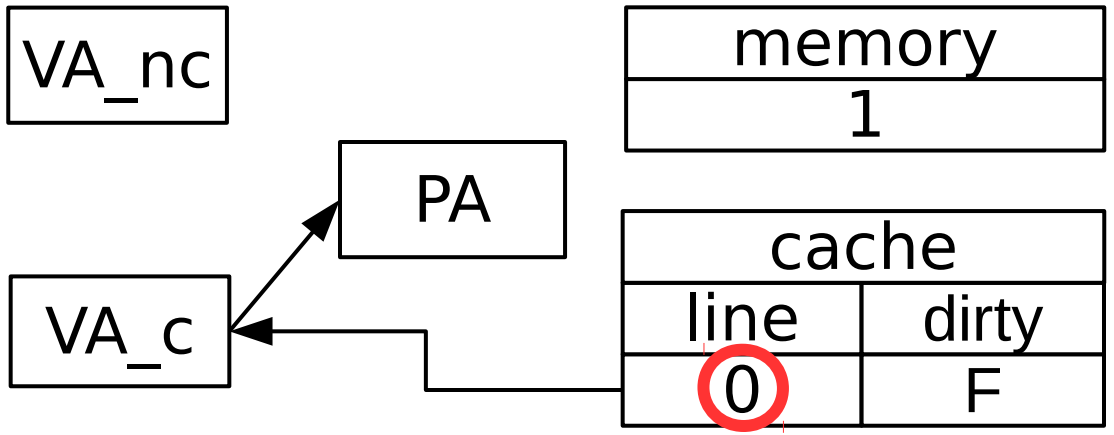

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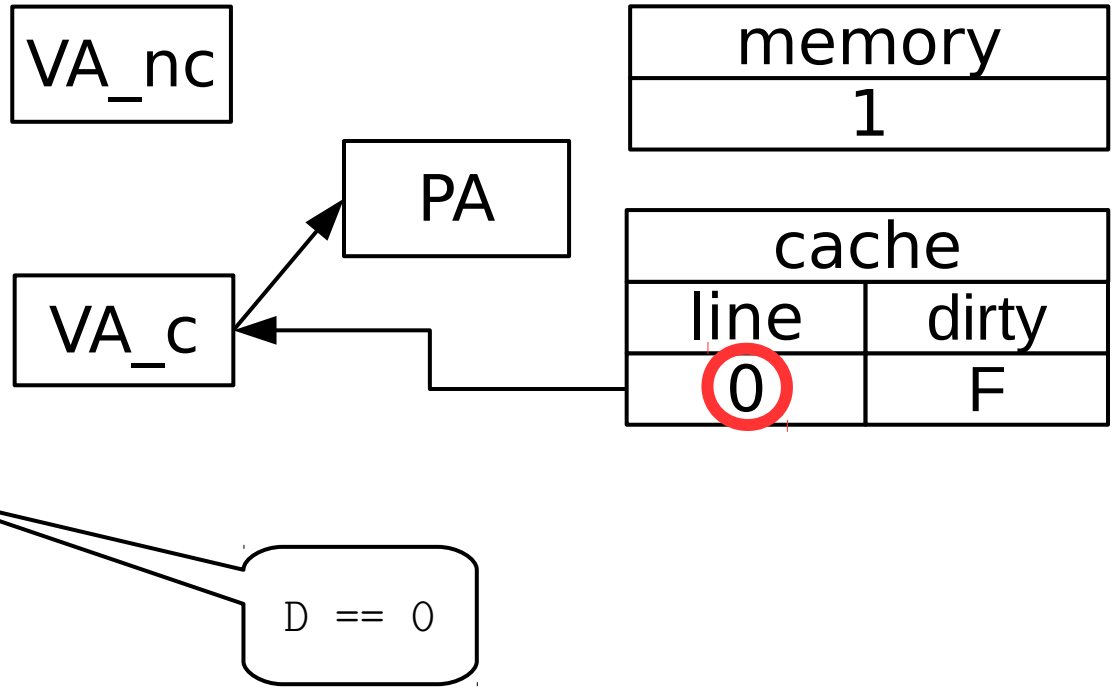

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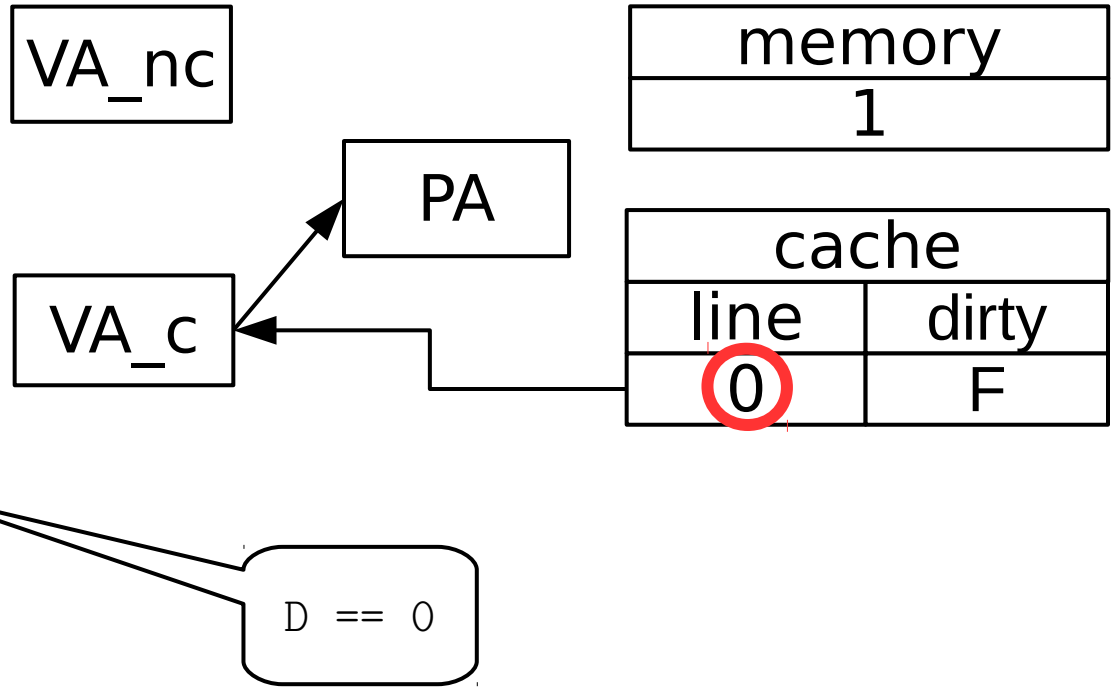

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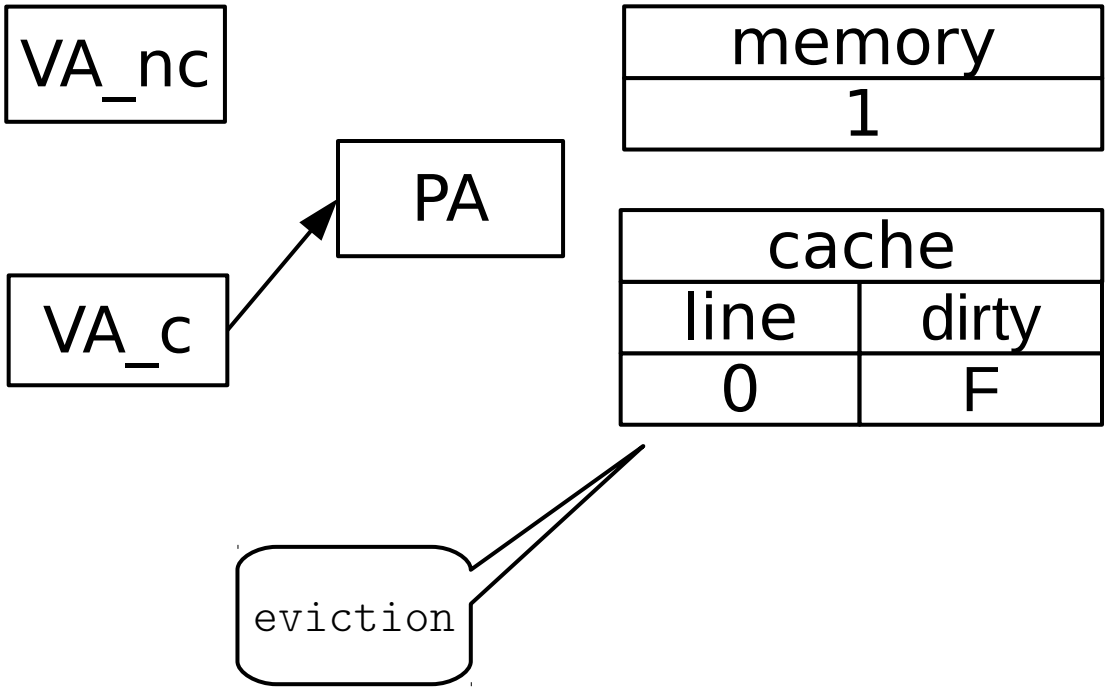

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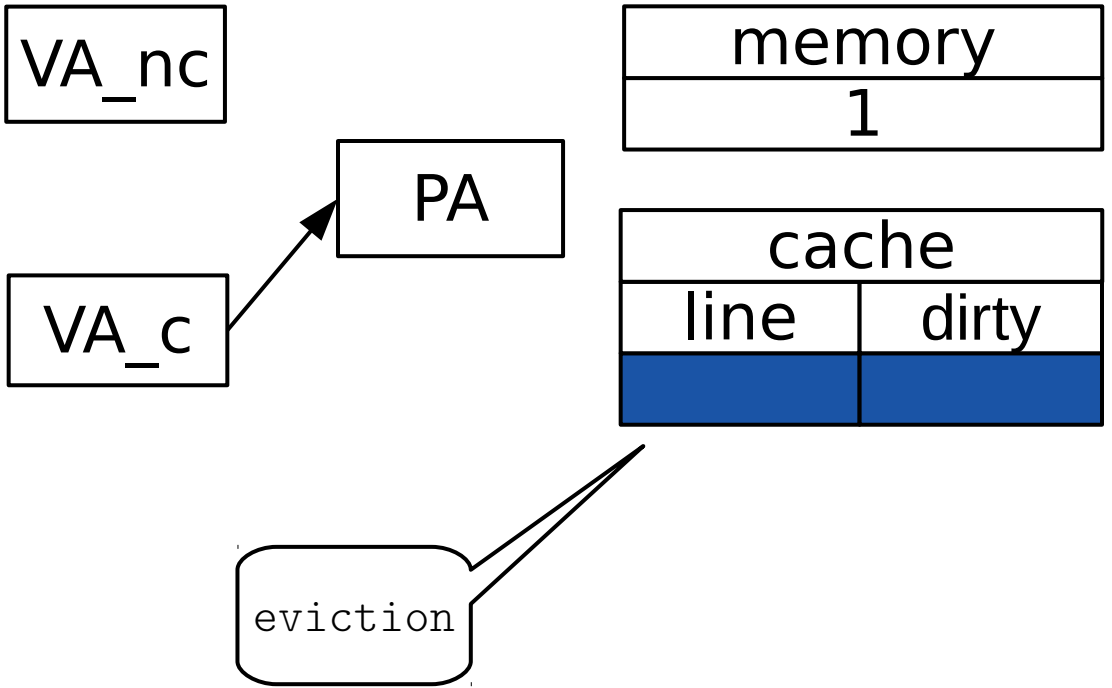

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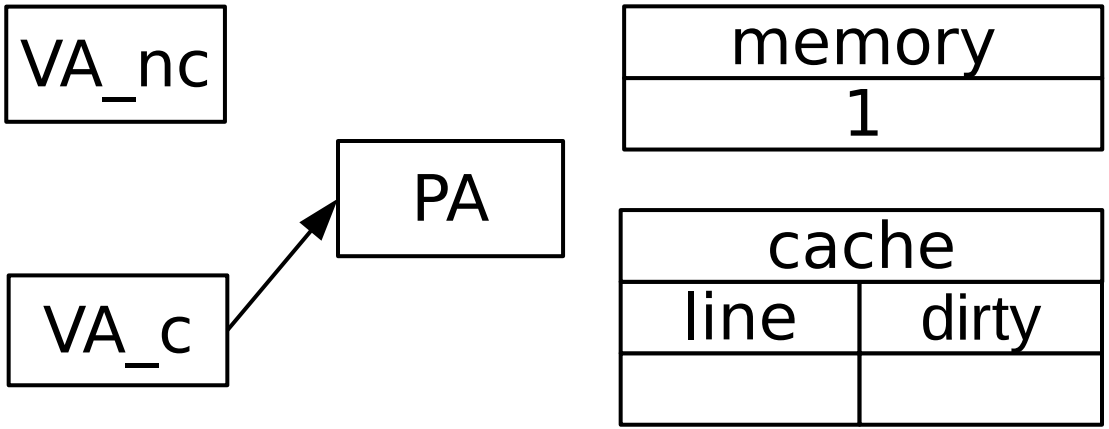

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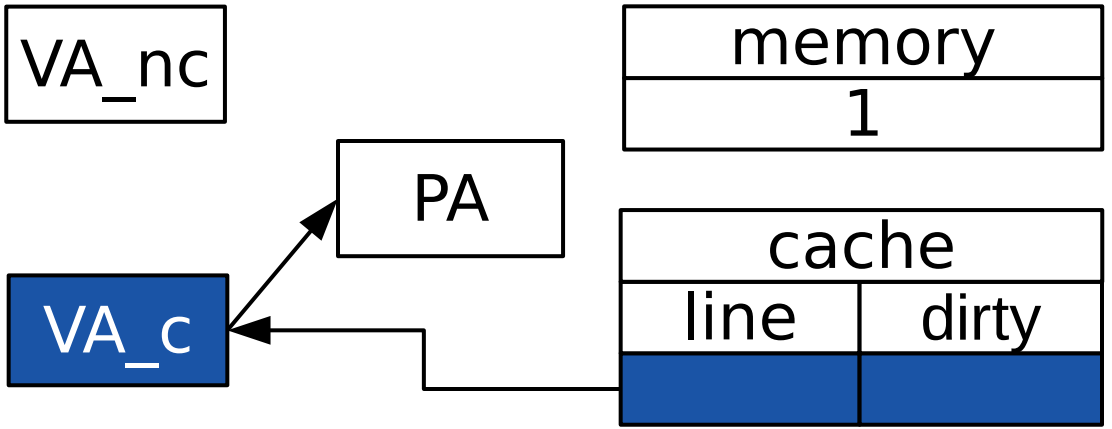

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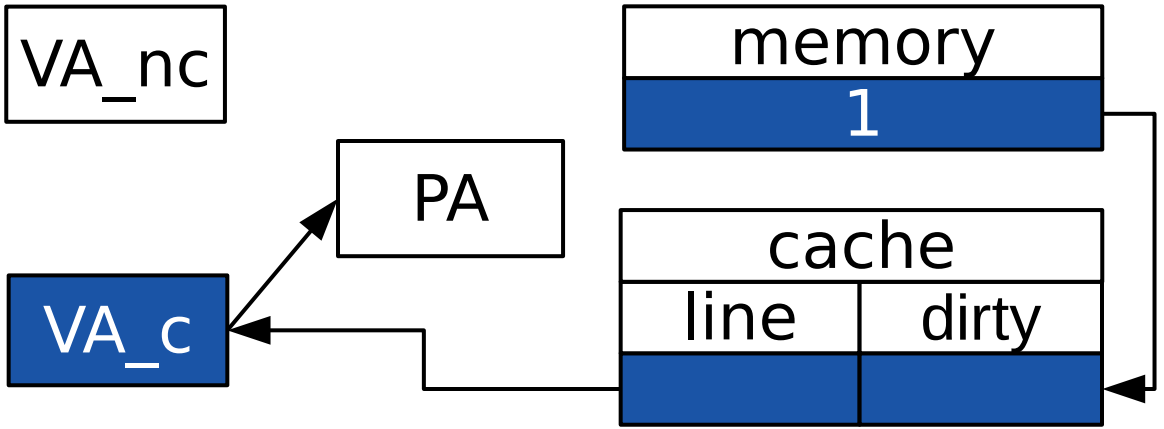

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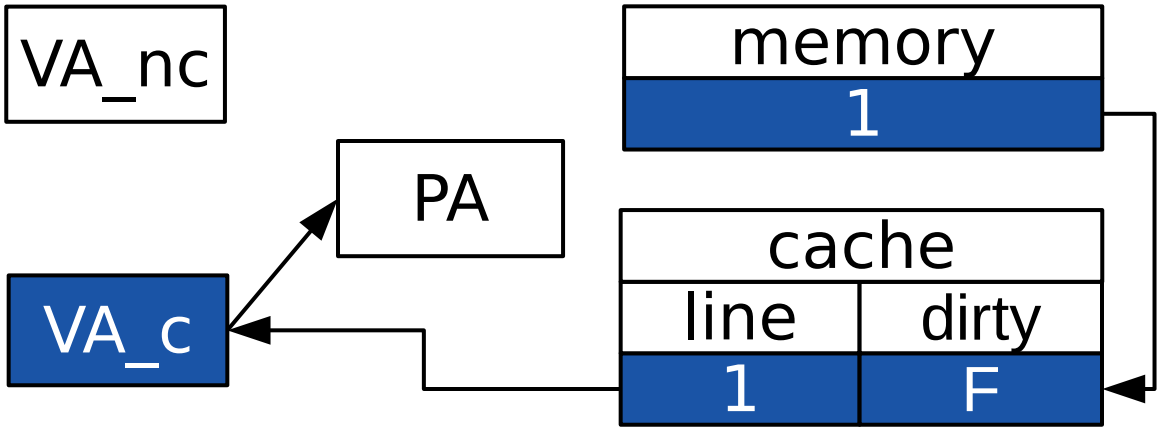

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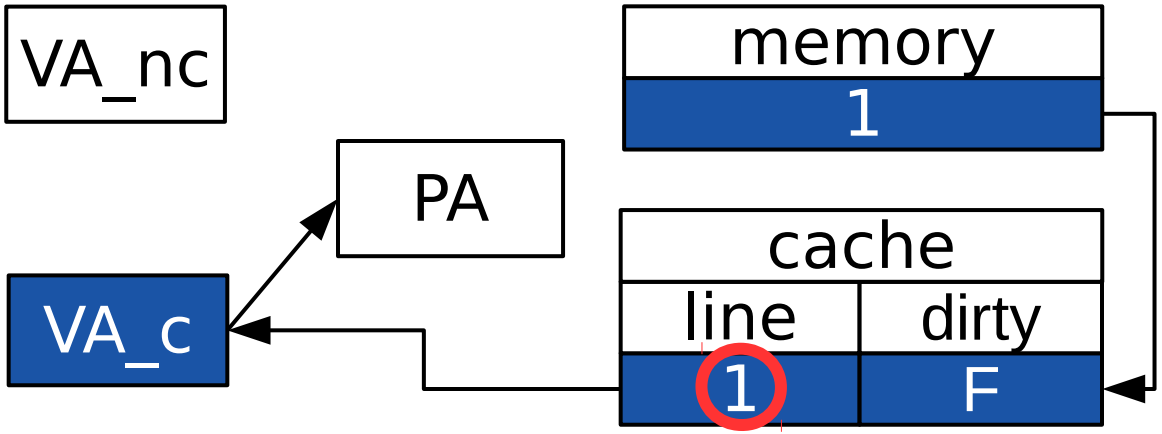


Storage channels

Integrity threat

- Transfer of memory ownership
- Time Of Check To Time Of Use attacks
- No need of
  - simultaneous double mapping
  - concurrency

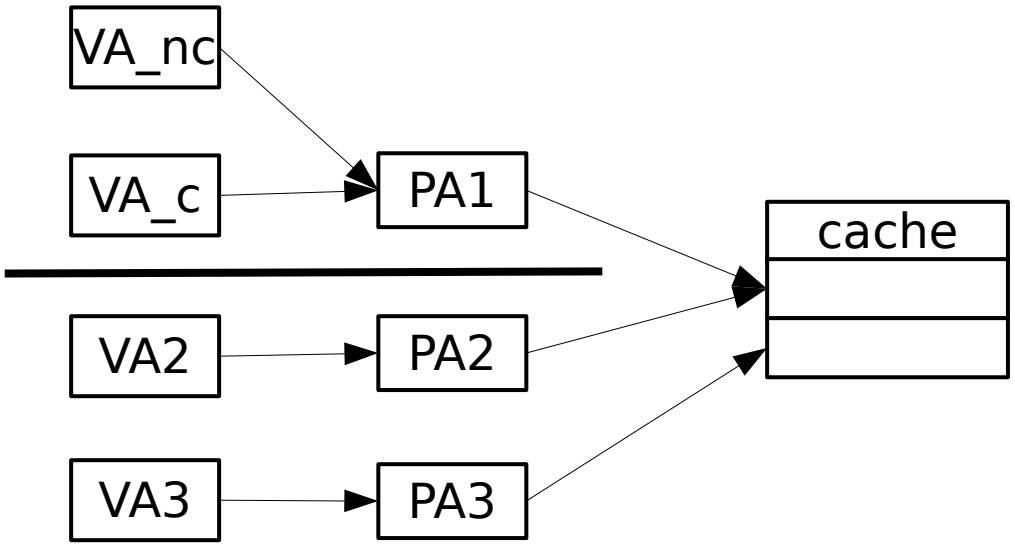
Natural preys: reference monitors

Attacker

```
invalidate(VA_c)
write(VA_nc, 0)
D = read(VA_c)
write(VA_nc, 1)
call victim
D = read(VA_c)
```

Victim

```
if secret
   access(VA2)
else
   access(VA3)
```



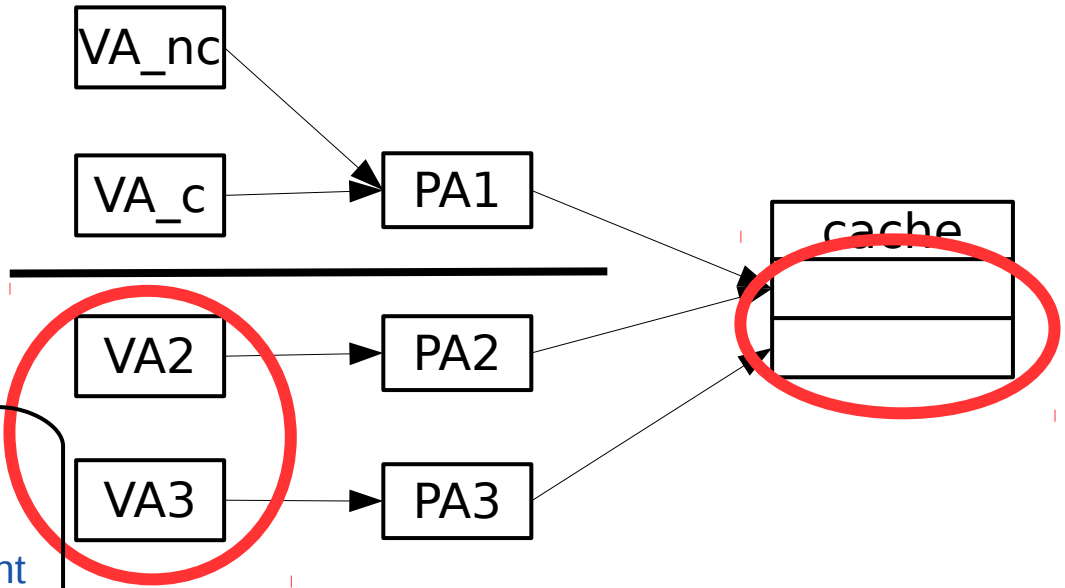
Attacker

```
invalidate(VA_c)
write(VA_nc, 0)
D = read(VA_c)
write(VA_nc, 1)
call victim
D = read(VA_c)
```

Victim

```
if secret
   access(VA2)
else
   access(VA3)
```

Accessed cache line is secret-dependent



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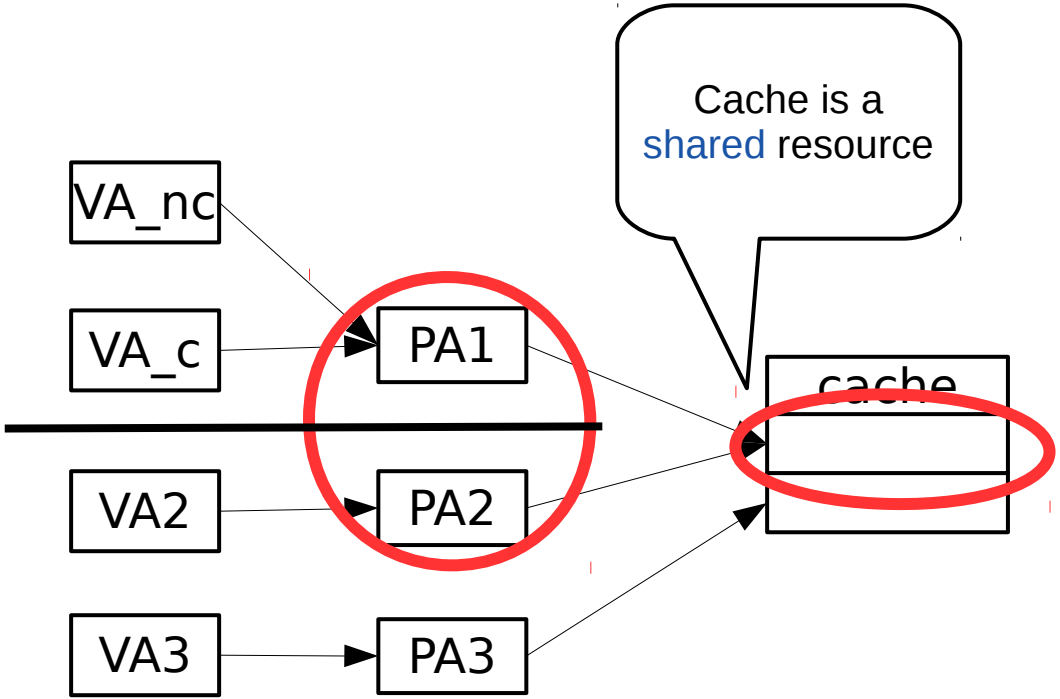

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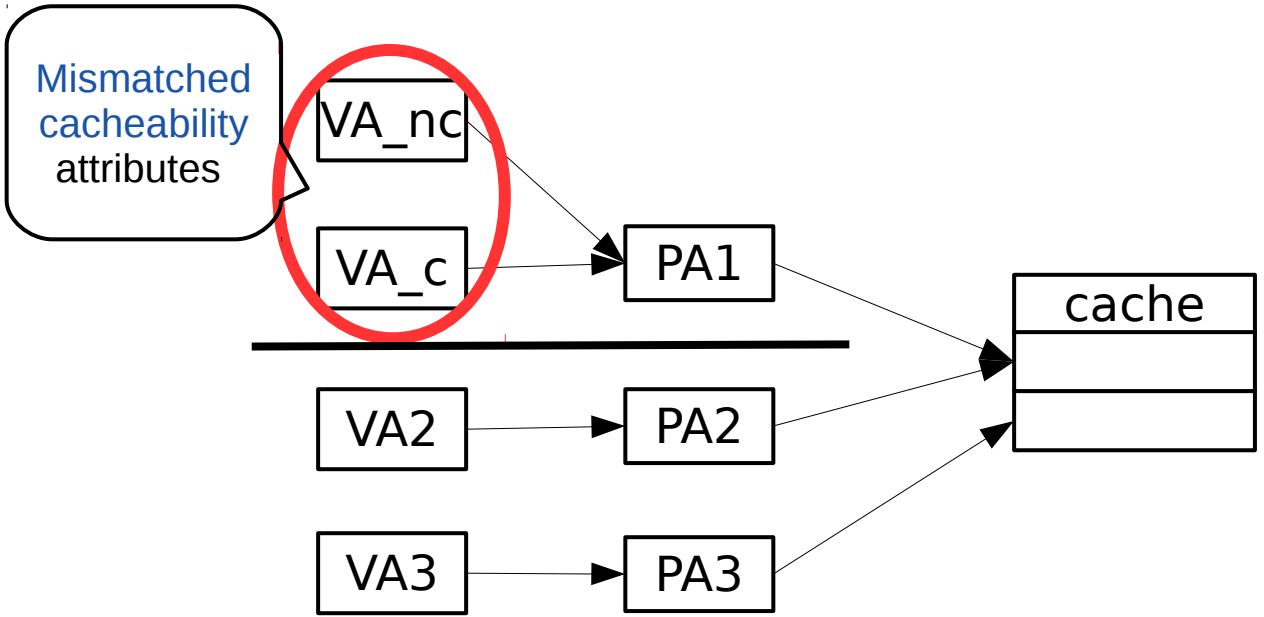


Storage channels

Integrity threat

- Transfer of memory ownership
- Time Of Check To Time Of Use
- No need of
  - simultaneous double mapping
  - concurrency

Natural preys: reference monitors

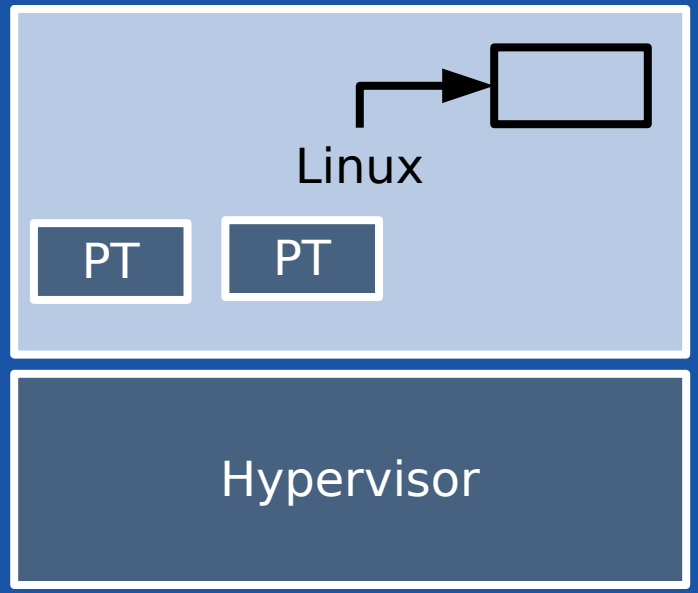
Confidentiality threat

- Access driven attacks
- No external measure needed
- Difficult to counter-measure at probing time

Natural preys: look-up tables

Paravirtualizing Hypervisor

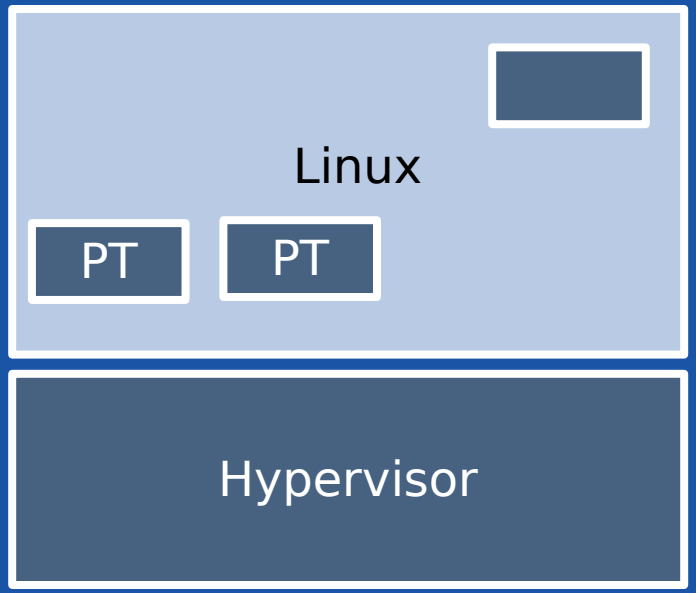
- Beagleboard



Linux prepares a PT

Paravirtualizing Hypervisor

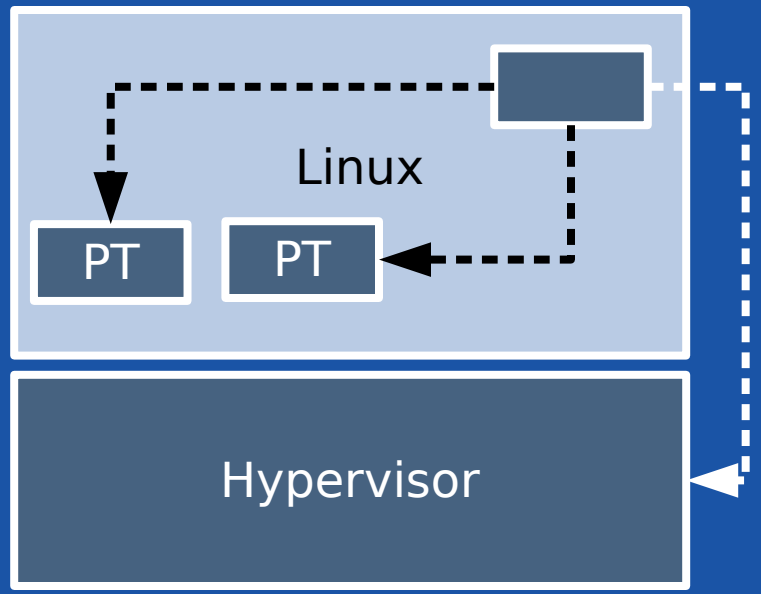
- Beagleboard



Hypervisor makes region read-only

Paravirtualizing Hypervisor

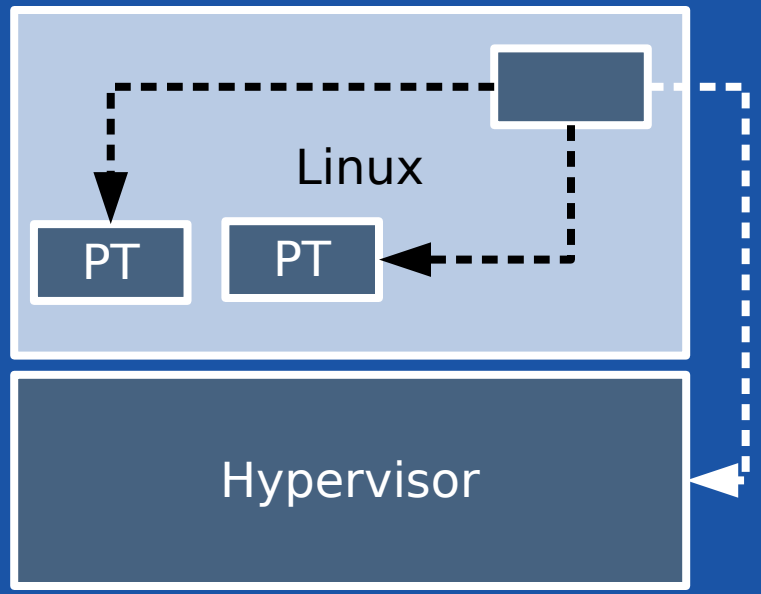
- Beagleboard



Hypervisor validates content

Paravirtualizing Hypervisor

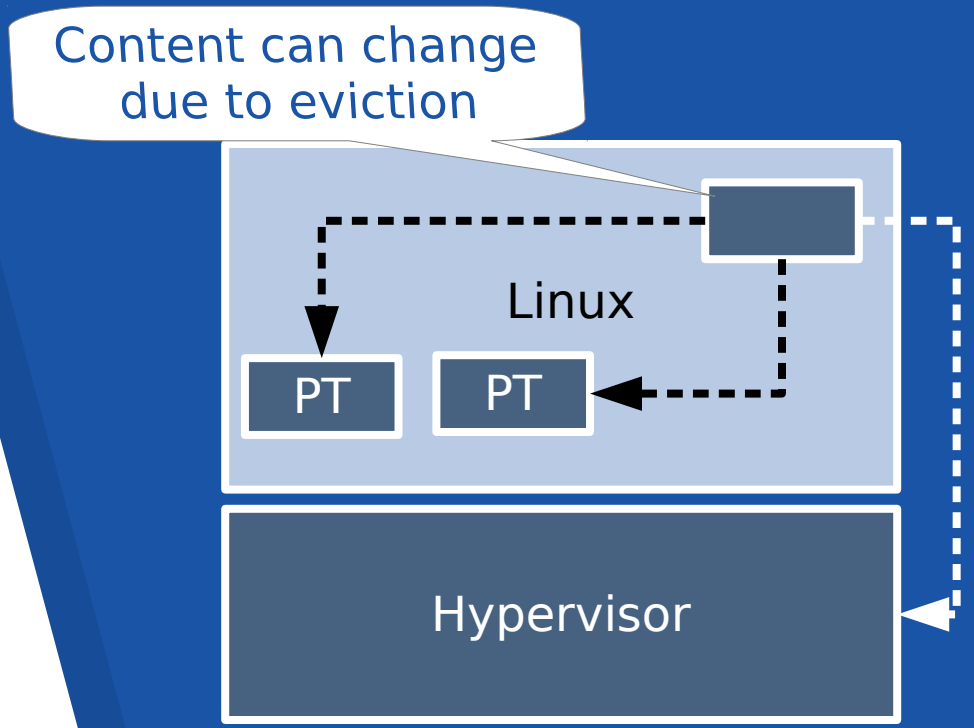
- Beagleboard



Hypervisor activates PT

Paravirtualizing Hypervisor

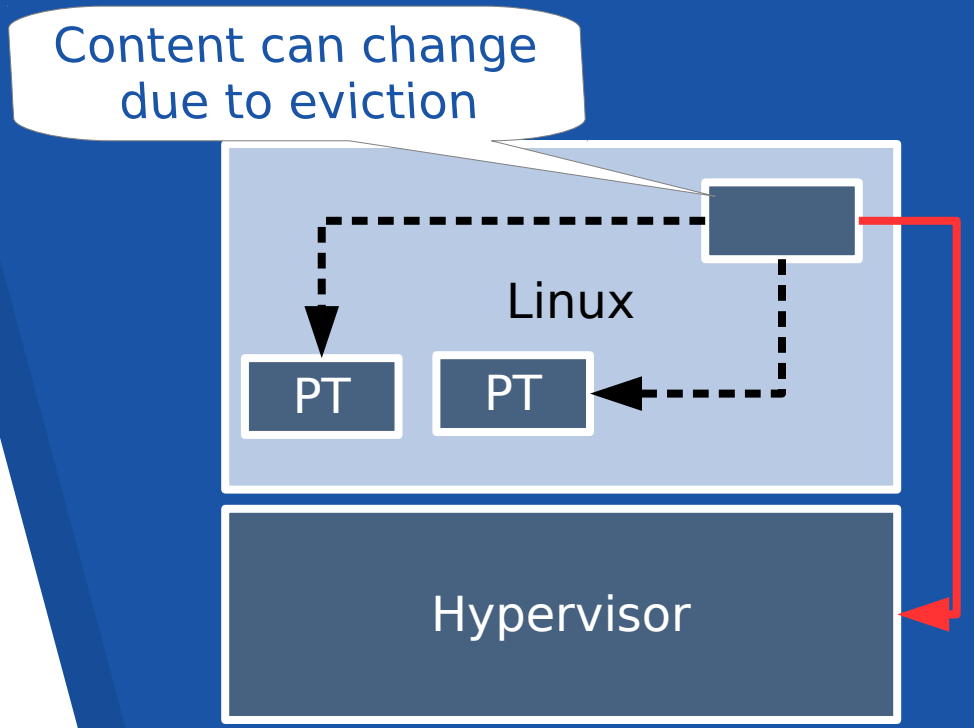
- Beagleboard



Hypervisor activates PT

Paravirtualizing Hypervisor

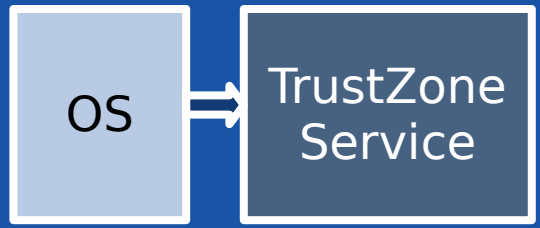
- Beagleboard
- Linux takes complete control



Hypervisor activates PT

AES Cryptoservice

- Raspberry PI 2
- 128-bit key extracted after 850 encryptions



Vulnerability:

c[j]=Kn[j] xor T4[s[j]]

Observable

Inferred

Countermeasures

Integrity threat
guarantee memory coherency

- cache flushes
  (8x overhead)
- selective eviction
  (0.2x overhead)

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  (5x overhead)
- no cache for secret accesses
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HW Countermeasures

- do not disregard
  unexpected cache hit

Fixing Formal Verification

- Fix incoherent memory problem
- Verify countermeasures
- Property: Different memory/cache data for same VA means that cache line **must** be dirty

Questions