FLINT
Implementation and Testing

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Amended Specification

- SPARC V8 processor implementation
  - Optimized for the Virtex5 family of Xilinx FPGAs
  - Compact design with higher CPI
  - Tolerance for variable latency of major components
    - TLB, Memory, ALU, Register File, etc

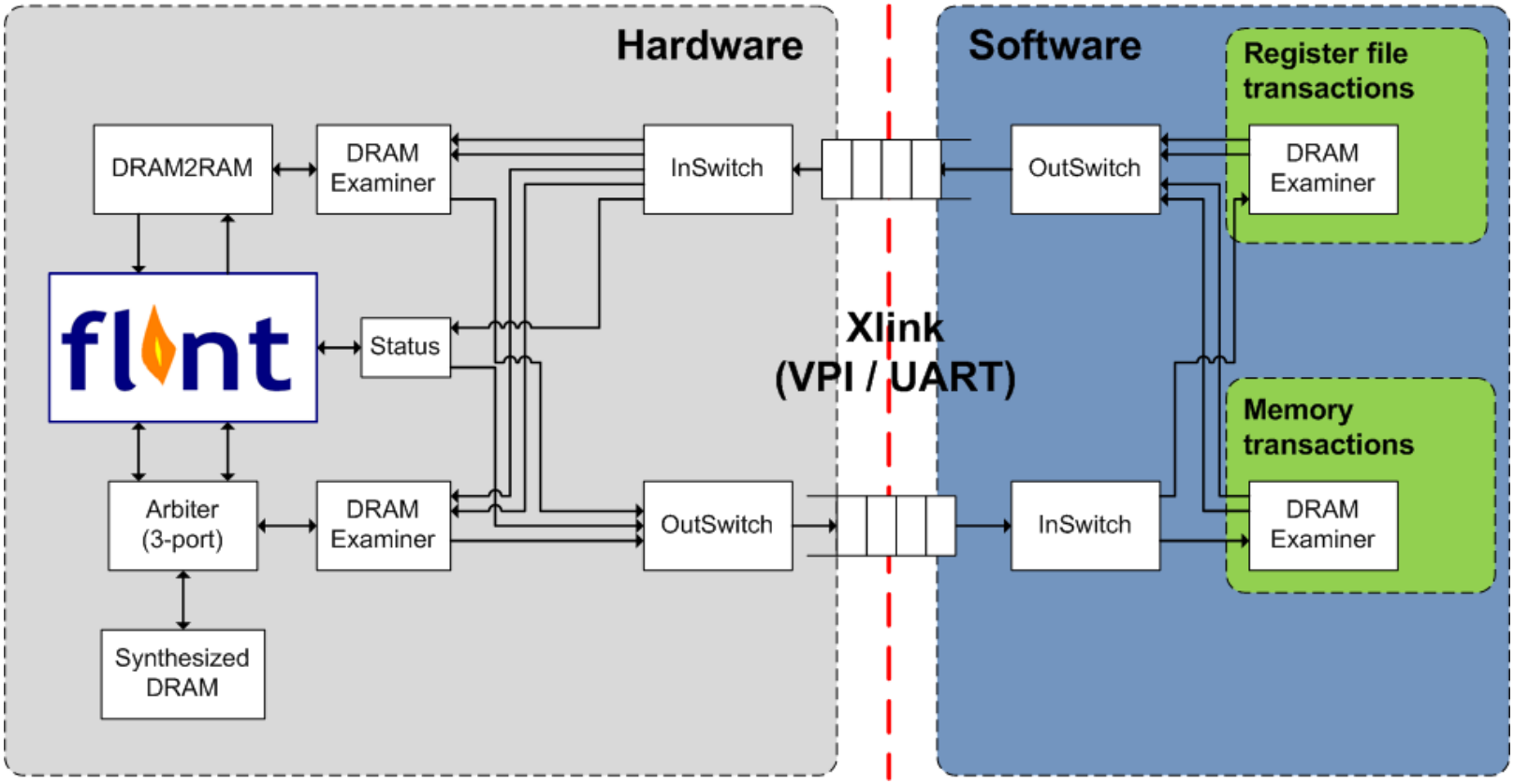
Progress (1)

- Completed components
  - Register file
  - ALU
  - “TOP” level datapath and control flow
  - Interface to RAMP DRAM backend memories
- Completed instructions
  - All add/sub/logical instructions

Progress (2)

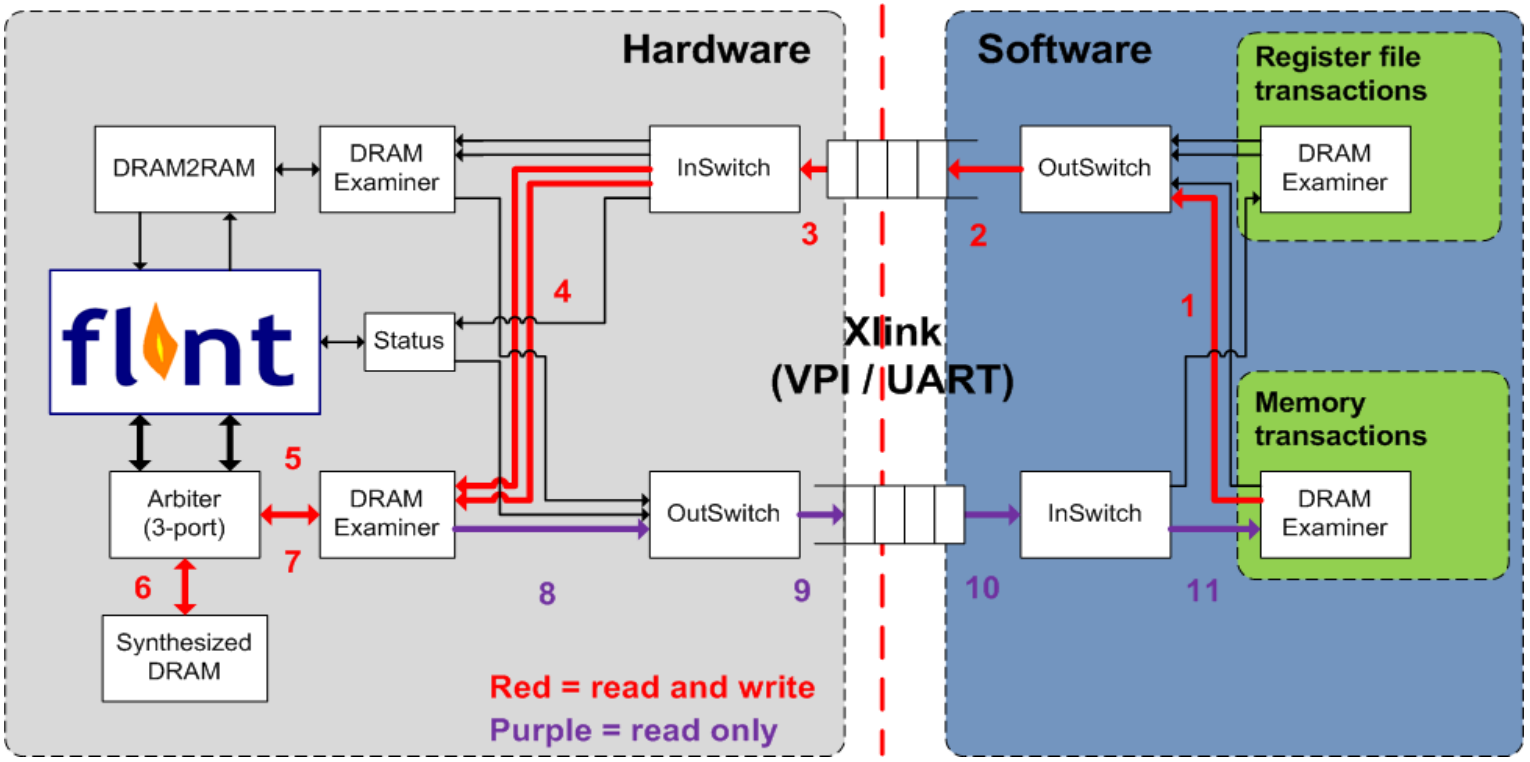
- Close to completion
  - XLink test framework
- Next step
  - Implement the remainder of the ISA
    - Test each new instruction in simulation and hardware automatically

Test Harness (1)



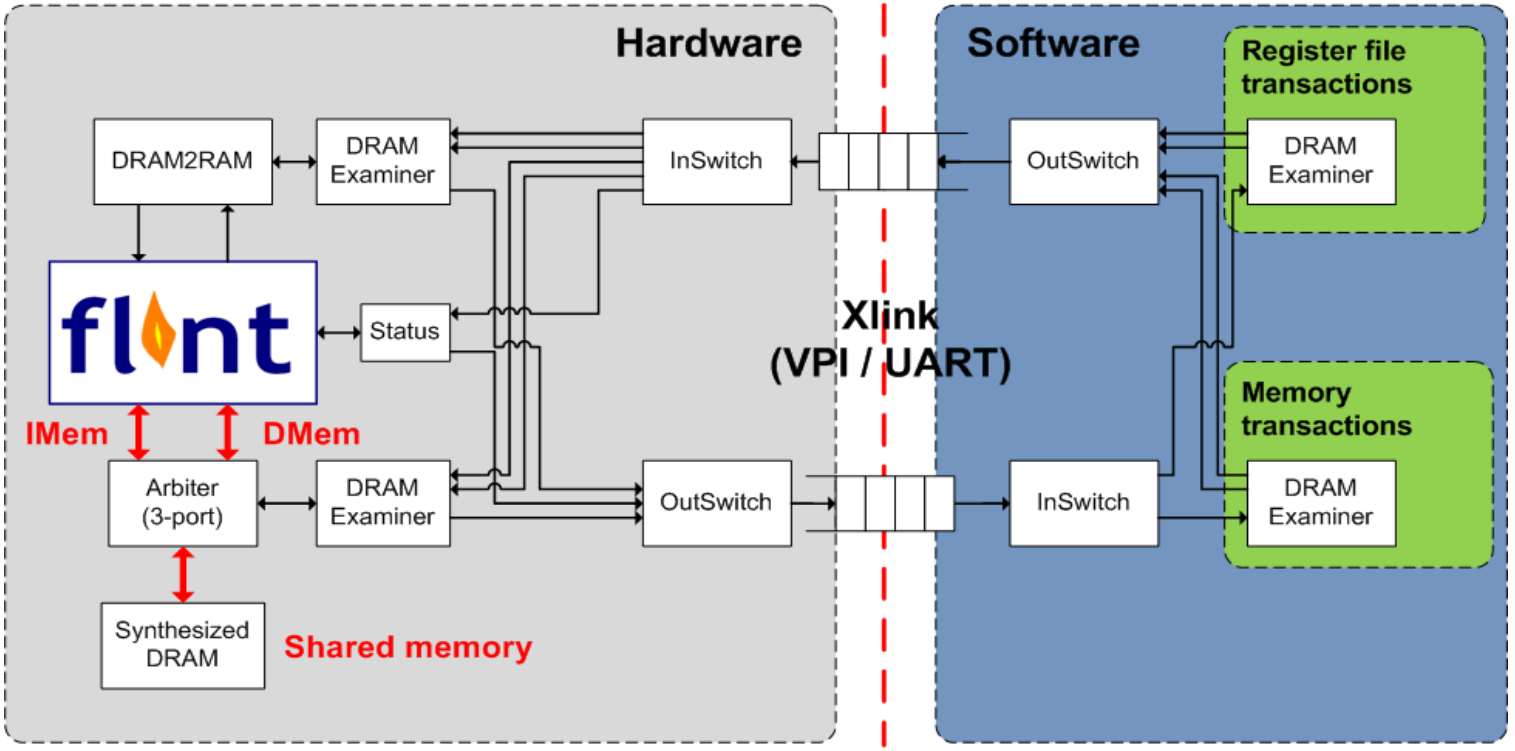
Test Harness (2)

- Example: write/read to/from memory



Test Harness (3)

- Example: processor to memory



Test Harness (4)

- Example: normal processor operation
  1. System reset → processor stalls
  2. SW loads processor memory and state
  3. SW says “Go”
  4. Processor executes loaded instructions
  5. Processor says “Done”
  6. SW reads processor state and memory

Test Harness Advantages (1)

- Minimize gap between Modelsim and Xilinx
  - Little to no change from simulation to hardware verification
- Connect processor to arbitrary memory backend

Test Harness Advantages (2)

- Test procedure **(one button click)**
  1. Write assembly code
  2. Pass through RAMP GOLD functional SPARC simulator
  3. Pass through FLINT in simulation
  4. Compare #2 and #3
  5. Pass through FLINT in hardware
  6. Compare # 2 and #4